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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/903,453	07/29/1997	LEONARD FORBES	303.378US1	2271

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EXAMINER
ECKERT II, GEORGE C

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/21/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
08/903,453	Forbes et al.
Examiner	**Art Unit**
George C. Eckert II	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Mar 21, 2002*.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *2, 3, 24-28, 41-48, 50-52, and 65-68* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *2, 3, 24-28, 41-48, 50-52, and 65-68* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 33
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

1. Applicant's amendment dated September 5, 2001 in which claims 1, 4-6, 20-23, 29-40, 49 and 53-64 were canceled has been entered of record.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 2 and 3 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 11-18 of co-pending Application No. 08/902,843. Although the conflicting claims are not identical, they are not patentably distinct from each other because the present invention and co-pending Application no. 08/902,843 disclose a transistor having:

a source and a drain separated by a channel supported by a semiconductor substrate;

a floating gate formed between the source and the drain above the channel and separated by an insulative amorphous carburized silicon layer;

a control gate formed adjacent to and insulated from the floating gate;

wherein the transistor is part of a memory cell comprising a capacitor.

Further, stacked capacitors are well known and widely used in memory devices.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 U.S.C. § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 2, 3, 24-28, 41-48, 50-52 and 65-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakata et al., *Amorphous silicon/amorphous silicon carbide heterojunctions applied to memory device structures*, Electronics Letters, April 28, 1994, Vol. 30, No. 9 (of record), in view of JP 8-255878 to Sugita et al. (of record) and Burns et al., *Principles of Electronic Circuits.*

With regard to claims 2, 3, 24, 45, 46, 48, 50, 52, and 68, Sakata et al. teach in figure 1 the formation of an insulative layer of amorphous silicon carbide, shown as the a-SiC:H (graded)

layer, formed on top of a substrate which is crystalline silicon (c-Si) that can be p-type (see *Sample Preparation*);

a floating gate formed of amorphous silicon, shown as the a-Si:H layer, formed above the amorphous silicon carbide insulator,

a second insulative layer of amorphous silicon carbide, shown as the a-SiC:H layer, formed above the a-Si:H floating gate, and

a control gate shown as metal in figure 1 and later taught as aluminum (see *Sample Preparation*).

And though Sakata et al. teach that the above structure "can be applied to floating-gate memory devices[,]" Sakata et al. do not teach the structure further comprising a source region, a drain region, or a channel region therebetween. However, such regions are taught by Sugita et al. Specifically, Sugita et al. teach, with reference to figure 1, a floating gate memory device comprising:

an N+ type source region 2 and an N+ type drain region 3 (see page 11, paragraph 0032 of the translated reference which states that the source and drains 2 and 3 are n+ type);

the source and drain regions formed in a p-type silicon substrate (see page 2 of the translated reference which lists the reference numerals and corresponding elements and shows that numeral 1 represents a p-type silicon substrate);

a channel region between the source and drain regions in the substrate (though the channel region is not numbered, it is inherent that there exists a channel region between the source and

drain of a transistor, see *Principles of Electronic Circuits*, pp. 382-83 shows an n+ source and an n+ drain in a p-type substrate and refers to the device as one comprising an "n-channel");

a floating gate 6 (see page 3 of the translated reference and the list of elements which labels numeral 6 as a polysilicon floating gate) which is formed above and insulated from the substrate;

a control gate 8 formed above the floating gate and separated from the floating gate by a dielectric layer 7 (again, see the list of elements on page 3 of Sugita et al. where element 8 is labeled a control gate and element 7 is listed as SiO_2, a known, inherent insulator).

Sakata et al., Sugita et al. and Burns et al. are combinable because they are from the same field of endeavor, which field is the formation of floating gate devices. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form a source region, drain region and channel region in the device of Sakata et al. The motivation for doing so is that the source, drain and channel regions allow individual floating gate devices to be formed in an array. That is, by forming source and drain regions having the floating gate stack therebetween, a plurality of floating gate devices can be formed in one substrate and yet be individually written and erased by the use of the source, drain and channel regions. The use of the source/drain/channel regions for such programming is well known in the art. For example, Burns et al. explicitly teach such programming steps in the paragraph bridging pages 382-83. Furthermore, Sugita et al. generally teach this integration concept in paragraphs 0001 - 0005 of

the translated reference. Therefore, it would have been obvious to combine Sakata et al with Sugita et al and Burns et al. to obtain the invention of claims 2, 3, 24-28, 41-48, 50-52 and 65-68.

Regarding the use of polysilicon as the material for the control gate, Sakata et al. indicate that the control gate is formed of aluminum while Sugita et al. are silent as to the material for their control gate. However, Burns et al. teach on page 382 that control gates (or, as there labeled, select gates) are typically formed of polysilicon. Even beyond the teaching of Burns et al., the use of polysilicon as a control gate is considered well known in the art. There are several advantages of using polysilicon as a control gate, for example, polysilicon can be doped to a low resistivity and is able to withstand higher temperatures so that it is unaffected during subsequent annealing steps. As such, it is considered obvious to form the control gate of Sakata et al. from polysilicon.

As to the method of formation of the insulation layer between the floating gate and the substrate from silicon carbide, Sakata et al. teach or in the alternative make obvious such a structure. The limitation that the amorphous carburized silicon is *grown* on the substrate is taught or in the alternative obvious over Sakata et al. In support of the process term *grown*, it is noted that applicant's *growth* method is a deposition (specification p. 6, lines 3-4). Sakata et al. also teach a deposition method (see *Sample preparation*). As such, Sakata et al.'s deposition process anticipates the growth process limitation as instantly claimed.

In the alternative, and with further regard to the limitation where the *growth* process is further limited to be a microwave PECVD, limitations in the instant claims as to the process by which the final product is achieved do not distinguish over that taught by Sakata et al. That is,

such limitations are product by process limitations. Note that a "product by process" claim or limitation is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that, once a product appearing to be substantially identical is found and a rejection is made, the burden shifts to the applicant to show an unobvious difference based on the claimed process steps. MPEP §2113. Instantly, because no evidence was proffered by applicant as to patentability based on the added process limitations, the burden remains with applicant to do so.

Response to Arguments

4. Applicant's arguments filed March 21, 2002 have been fully considered but they are not persuasive. Applicant's arguments focus on two principles: 1) the combination of references must be motivated or suggested by the references themselves or by that which is common knowledge in the art, *MPEP §2143*, and 2) if the proposed modification or combination of the references would change the principle of operation of the prior art invention being modified, then the teachings of

the references are not sufficient to render the claims *prima facie* obvious. *MPEP §2143.01.* However, neither of these arguments are persuasive for at least the following reasons.

As a preliminary matter, Applicant's statements in Response are conceded as to the recitations of claim 24: a transistor comprising a source region in a substrate, a drain region in the substrate, a channel region between the source region and the drain region in the substrate, and a gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate. And the majority of Applicant's statements as to the disclosure of Sakata are also conceded: that Sakata teaches a heterojunction structure comprising c-Si, a layer of hydrogenated amorphous silicon carbide (a-SiC:H), a layer of hydrogenated amorphous silicon (a-Si:H), another layer of a-SiC:H, and aluminum, and further that Sakata does not expressly teach a source region, a drain region or a channel region in a substrate. However, Applicant's additional statements as to the teaching of Sakata in figure 1 are not conceded. Specifically, Applicant states that Sakata teaches in figure 1 a heterojunction *diode* structure. This is too narrow a reading of what is there shown. That is, figure 1 is merely a band diagram of a heterojunction structure; but it in no way limits the application of the heterojunction structure to a diode. Actually, Sakata teaches, in the paragraph directly below figure 1, that "the HJ (heterojunction) structure shown in Fig. 1 can be applied to floating gate memory devices." Furthermore, Sakata teaches in the abstract (top of col. 1) that the heterojunction structure "can be applied to electrically programmable and erasable memory devices." Sakata does state that a "test diode," with the new heterojunction structure, was formed. However, this test structure cannot be construed to limit

the teaching of Sakata to only that structure. Rather the test structure is just that, a structure employing the HJ layers of the instant disclosure for purposes of testing their characteristics.

As to Applicant's first argument, it is argued, and here conceded, that motivation or suggestion to combine references must be found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. In the instant rejection, motivation and suggestion to combine the references is found in the explicit statements of the reference. Specifically, Sakata clearly states (page 688, first column, bottom paragraph) that the a-SiC:H/a-Si:H heterostructure "can be applied to floating-gate memory devices." Sugita teaches such a floating gate device. Applicant must surely agree that a suggestion to combine could not be more clearly announced.

But Applicant does not agree. Rather, Applicant argues in Response that "Sakata is **not** here stating that the HJ structure is a floating gate transistor, but may be merely expressing the hope that the HJ diode structure can be used in some unspecified type of memory device." This is not persuasive as it is twisting the teaching of Sakata into something that it clearly is not. Rather, as opposed to Applicant's interpretation that Sakata can but merely hope for application of the HJ structure in some unspecified device, Sakata clearly suggests the application of the HJ structure to a "floating gate memory device." Sakata does this by simply stating "the HJ structure *can be applied to floating-gate memory devices.*" (*Emphasis added*). This is not a hope for application of the HJ structure in some "unspecified type of memory device" but a direct reference to use of the HJ structure in an established device, one that is well-known in the art. It is the same

structure taught by Sugita, the same structure taught by Burns and, for the record, the same structure taught by *Complete Guide to Semiconductor Devices* to Ng (pp. 322-28, 605-08) and the same structure taught by *Silicon Processing for the VLSI Era, Volume 2 - Process Integration* to Wolf (pp. 623-28). Floating gate memory devices are well known in the art, and they are *all* taught having a source, drain and channel.

In a similar light, Applicant first concedes that the C-V plot shown in figure 2 of Sakata does teach a large hysteresis that may be used as a memory window to create a device to store data, but then Applicant argues that this "is **not** a suggestion that the HJ diode structure of Sakata can be combined with the elements of the floating gate transistor of Sugita." First of all, this again too narrowly reads the teaching of Sakata as only a *diode* structure. Secondly, it simply ignores the function and operation of a floating gate device, including the one taught by Sugita. The function of a floating gate device *is* to store data. This is taught not only by Burns (p. 383, 1st full paragraph; "When the programming voltage is removed, the electrons on the floating gate are trapped," and thus the cell is programmed) but also by Wolf (p. 625, 1st full paragraph; "Once electrons are transferred to the gate, they are trapped there, as illustrated by the energy-band diagram shown in Fig 8-34."). As such, Applicant's statement that the teaching of Sakata cannot be considered a suggestion to combine the HJ structure with the additional elements of a floating gate transistor (such as that taught by Sugita), is simply not persuasive as it directly contradicts that which is expressly suggested by Sakata.

Applicant's second argument is that Sakata is not combinable with Sugita because the two devices operate differently. That is, while Sakata teaches that the HJ device is programmed by electron injection into the a-Si:H layer and erased by hole injection into the same layer to recombine with the electrons, Burns teaches that a typical floating gate device is not erased using holes. Therefore, according to Applicant, the different operations of the two references denies their combination. However, there are at least two reasons why this argument is not persuasive.

First, it is not dispositive that Burns does not mention holes in the erase process of a floating gate device. Especially in light of the teachings of Wolf. Specifically, Wolf, on pages 625-26 explains the program and erase mechanisms of a floating gate device. There, Wolf teaches that, like the devices of Sakata, Sugita and Burns, a floating gate device is programmed by electrons stored on the floating gate by the creation of hot electrons near the drain which electrons traverse the oxide (gate insulator) and charge the floating gate. Wolf also teaches that to erase the cell, as in the teaching of Burns, UV light is applied to the gate. However, unlike Burns which only states that the UV light imparts energy to the electrons which allows them to escape, Wolf gives a better explanation of the mechanism. Specifically, Wolf teaches that "the UV light creates electron-hole pairs in the SiO_2, providing a discharge path for the charged floating gate." As such, electrons and holes are both involved in the erase process of a floating gate device.

Second, regardless of the mechanism of charge storage or erasure, the combination of the references does not change the principle of operation of either device nor negate the combination

itself. That is, Sugita was relied on merely for teaching the use of source, drain and channel regions. The addition of these regions in the device of Sakata will not alter the manner in which electrons are stored or erased. Rather, as made clear in the rejection, the use of source, drain and channel regions simply facilitates the use of the HJ structure in an array. Specifically, a floating gate device is formed such that the floating gate is located between a source and drain, with the channel therebetween. By this arrangement, voltage may be applied to selected sources and drains to charge or program an individual cell. This is well known in the art and taught by Burns, as well as by Ng and Wolf. For example and as pointed out in the rejection, Burns teaches on page 383 that an individual cell is programmed by application of voltage to form a channel region between a source and drain, and from that channel electrons are excited and gain enough energy to charge the floating gate. Such use of a source and drain to supply electrons does not alter the principle of operation of the Sakata device.

Furthermore, the connection of a standard floating gate cell is shown by Burns in figure 9.10(a) on page 382. There, an individual cell is shown in a typical array configuration, where the word line is connected to the control gate, the bit line connected to the drain, and the source is grounded. It is by the use of a source, drain and channel, such as that taught by Sugita, that the HJ structure of Sakata can be arranged and used in an array, which array is then used to store data. These teachings - the use of a source, drain and channel regions - do not alter the principle of operation of Sakata's HJ device. Rather, with the use of a source, drain and channel, a great number of floating gate cells, wherein each cell stores one bit of data by individual charging or

discharging, can be arranged in rows and columns to thereby store a great deal of data. Such is taught by Burns (p. 383, last para., a 256k memory array of floating-gates transistors).

Applicant finally argues that the motivation to combine the references is insufficient to maintain the rejection. Specifically that the requirements set forth by the Federal Circuit in *In re Sang Su Lee* are not met. However, this is not persuasive as the requirements there set forth have been satisfied. As stated by Applicant, in *Lee*, the court required that the suggestion or motivation to combine references must be based on objective evidence of record and that the factual question of motivation is material to patentability and cannot be resolved on subjective belief and unknown authority. In this light, Applicant argues that such authority was not provided in the rejection and is not well known in the art. However, this ignores the fundamental nature of floating gate devices as taught by the Burns reference, cited in the rejection.

The motivation for combining Sakata, Sugita and Burns was that the use of source, drain and channel regions allow individual floating gate devices to be formed in an array. . . .[t]he use of the source/drain/channel regions for such programming is well known in the art." With this, Applicant takes issue. However, it is this that is clearly taught by Burns. Burns teaches that the source and drain are used to create electrons which are stored on the floating gate (p. 383, "electrons are accelerated in the high field between source and drain, and acquire enough energy to enter the conduction band of the gate oxide layer."). Burns further shows in figure 9.10(a) a floating gate device having source and drain connections and configured as an individual cell in an array. Finally, Burns teaches an example of such an array on page 383 - the 256k Intel chip which

uses an array of floating gate devices. If anything is missing from the references cited in the rejection, it is a picture showing an array of individual floating gate devices, each cell having a source, drain and channel, and configured in rows and columns of an array. However, such an arrangement is well known in the art and is not based on subjective belief or unknown authority. Rather, such an array is shown by several text book references, including Burns page 380 (figure 9.7, and see page 383, "The MOSFET cell in Fig. 9.7 is replaced by a floating gate transistor or stacked-gate cell as shown in Fig. 9.10(a).") and Ng, page 608, figure C6.5, as well as several of the patent references cited by Applicant including US 5,623,442, fig. 4B; US 5,912,837, fig. 4 & col. 4, lines 41-47; US 6,144,581, fig. 11; US 5,317,535, figs. 1 & 2, and text beginning in col. 3, line 28; and finally, US 5,740,104 to Applicant, figs. 1-3, and text in column 4, lines 57-59. In all, to say that it is not well known to form several devices in an array, each device having a source, drain and channel to facilitate individual programing, simply ignores that which is taught by Burns, and that which is well known in the art.

In fact, it is only Sakata that provides an example of a device that does not explicitly have a source, drain and channel. But again, Sakata teaches that the device as formed is only a *test* device; its purpose being to test the electron storage and thus memory capability between the a-SiC:H layer and the a-Si:H layer. Such testing was important to Sakata based on the leakage problems of previous devices. Specifically, Sakata teaches that "Capasso et al. reported similar memory devices based on AlGaAs/GaAs HJ. However, excessive leakage current made it impossible to electrically erase the memories. . . ." A review of the Capasso et al. reference

indicates clearly that their device was formed with a source and drain (see page 377, column 2, second full paragraph). This provides yet another teaching of a memory device in which a source and drain are formed.

In all, Applicant's arguments are not persuasive. The argument that there is no suggestion to combine the references is clearly refuted by the explicit suggestion of Sakata which states that the HJ structure can be applied to floating-gate memory devices. The argument that the proposed modification would change the principle of operation of the Sakata device is not persuasive because the addition of a source, drain and channel to the device of Sakata in fact would not alter its principle of operation. Finally, the motivation to use a source, drain and channel in the device of Sakata to allow the formation of the device in an array for a memory structure, is found not only in the teachings of Burns, but is well known in the art and not based on subjective belief or unknown authority.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (703) 305-2752.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Eddie Lee can be reached on (703) 308-1690. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

GCE
June 20, 2002

GEORGE C. ECKERT II
PATENT EXAMINER